

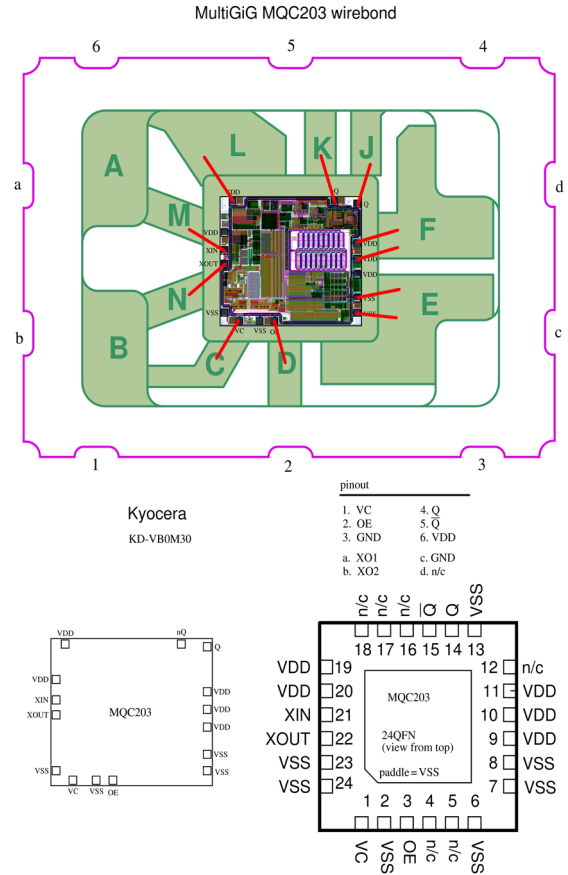
## 3.3V LVDS, LVCMOS, HCSL or LVPECL Voltage Controlled Crystal Oscillator with Multiplying PLL

### Product Description

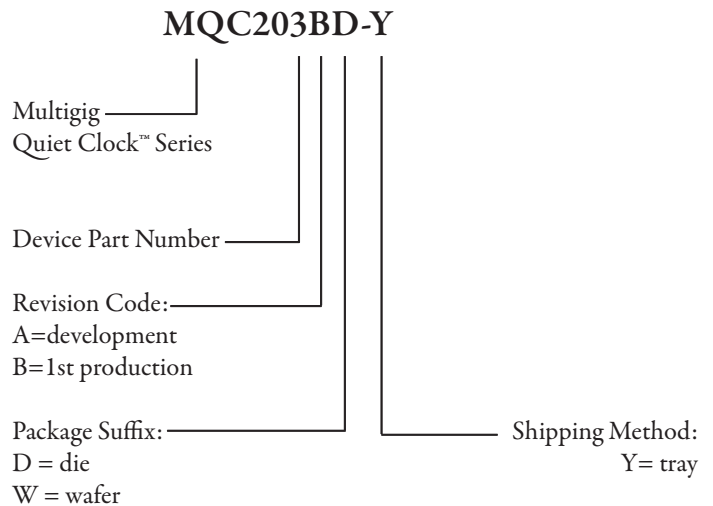
The MQC203 is a member of the Multigig QuietClock™ Series of low-noise timing solutions. Intended for use in 5×7mm oscillator packages, the MQC203 PLL multiplies the crystal to higher frequencies with typical jitters < 300fs in a 12kHz to 20MHz bandwidth. The VC pin allows control of the output frequency with a pull range between ±100 ppm and ±200 ppm with a typical linearity of ±4%. The MQC203 is user configurable via one-time programmable (OTP) memory. The outputs may be programmed to be one of LVDS, LVPECL, HCSL, or LVCMOS. An OE input is provided, and is programmable to be active high or active low. Crystal load capacitors are integrated on the die, and may also be programmed. The PLL feedback divider, VCO range, and output divider are set by OTP memory, and determine the VCO frequency and output frequencies. Kvcv linearity may also be trimmed. Output frequencies from 12MHz to 217MHz are available.

### Features

- Ultra-low Jitter, <300fs (12kHz - 20MHz)
- Common 8pf C<sub>L</sub> crystals
- LVDS, LVPECL, HCSL, or CMOS outputs
- Output frequencies of 12-217MHz
- Serial Interface for OTP via Q output and Vc
- Low voltage operation VDD = 3.3V ± 10%
- Industrial Temperature Range is standard (-40 to 85°C)
- Duty Cycle 48-52%
- Crystal drive level < 250uW
- Tuning Linearity ±4% typical, after trimming via OTP
- Pull Range: ±100 ppm Min.
- No downbonding required to configure the part



MQC203 Part Number:



MQC203 Block Diagram

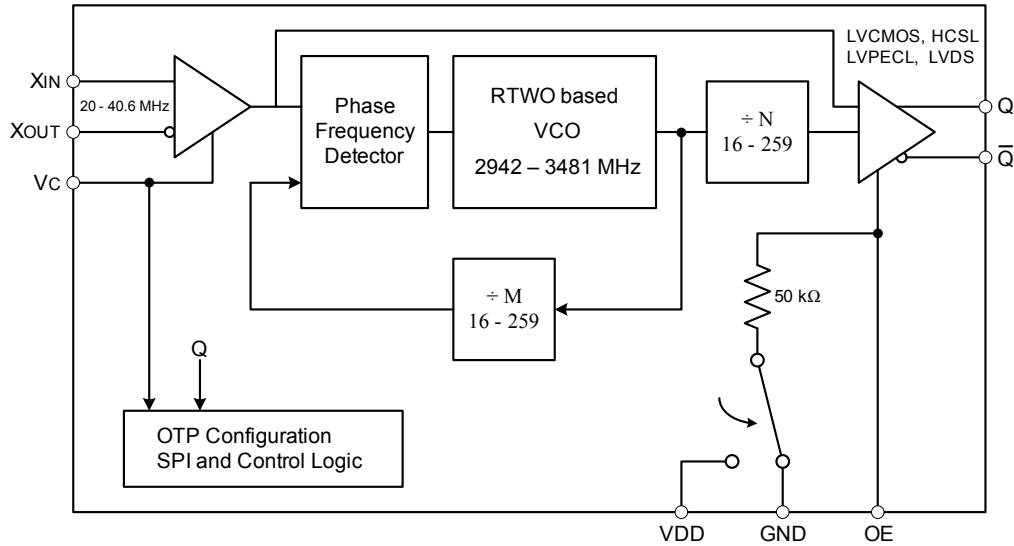
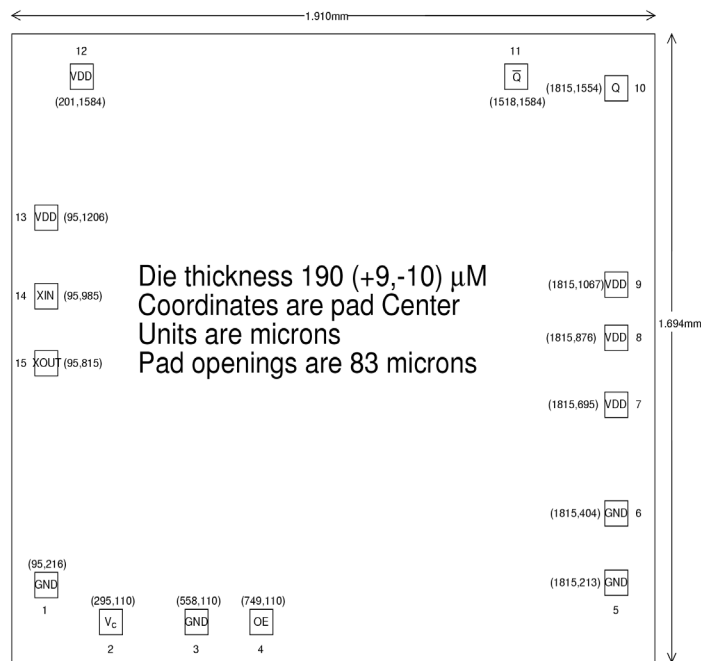


Figure-1

Pad coordinates



Multigig recommends bonding two GND and two VDD pads if possible. Only one of each of the VDD and GND pads must be bonded.

## Pin Description

Pin #	Name	Type	Level	Description
4	OE	See OE table	LVC MOS	See OE table
2	V <sub>C</sub>	Input	Analog	Control Voltage of output frequency also used for programming
10	Q	Output		Differential output (or LVC MOS output) also used for programming
11	$\bar{Q}$	Output		Differential output (or Hi-Z if LVC MOS is selected)
1, 3, 5, 6	GND	Power		Power
7-9, 12-13	VDD	Power		Power
14	XIN	To Crystal	Crystal	Connect to Crystal
15	XOUT	To Crystal	Crystal	Connect to Crystal

NOTE: Only 1 VDD and 1 GND must be bonded. Multigig recommends bonding 2 VDD and 2 GND pads.

OT [1:0]		Output Type
0	0	LVC MOS
0	1	LVDS
1	0	LVPECL
1	1	HCSL

OE invert OEC [1]	OE type OEC [0]	OE pin	Output State
0	0	0 or float/NC	Tristate
0	0	1	Enabled
0	1	0	Tristate
0	1	1 or float/NC	Enabled
1	0	0 or float/NC	Enabled
1	0	1	Tristate
1	1	0	Enabled
1	1	1 or float/NC	Tristate

OEC[1] controls the active state of the OE pin.

OEC[0] determines whether the OE pin is a pullup or pulldown. Program OEC[1:0] to 10 to enable outputs when the OE pin is at GND or unconnected.

VCO range [2:0]	VCO min	VCO max (MHz)
0 = 000	3321	3481
1 = 001	3202	3354
2 = 010	3098	3245
3 = 011	3007	3137
4 = 100	2942	3070

Output frequency = VCO frequency / opdiv [7:0].

VCO frequency = Crystal frequency \* fbdiv [7:0], and the VCO must be in one of the above ranges. Example: 155.52MHz. Select VCO range=2, and operate the VCO at 3110.4 MHz. Select a 38.88 MHz crystal. Fbdiv=80=3110.4/38.88. Opdiv=20=3110.4/155.52. See page 10 for more details and examples.

## Absolute Maximum Ratings

Symbol	Characteristics	Min	Max	Unit	Condition
VDD	Supply Voltage		4.6	V	
VIN	Inputs except V <sub>C</sub>	-0.50	VDD + 0.5	V	
V <sub>C</sub>	V <sub>C</sub> Input	-0.50	5.8	V	
VOUT	Outputs	-0.50	VDD + 0.5	V	
TA	Operating Temperature Range	-40	+85	°C	Industrial
TS	Storage Temperature Range	-65	+150	°C	

**NOTE:**

*Exposure to stresses at or beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device and may affect product reliability. These are absolute maximum specifications only, and functional operation of the device at these conditions or any conditions beyond those listed is not implied or recommended.*

## MQC203 ESD and Latch-Up Table

Test Item	Test Method Reference Standard	Condition
Electrostatic Discharge (ESD)	HBM (Human Body Model) JESD22-A114	Class 2: Passed 3000 volts
	MM (Machine Model) JESD22-A115	Class B: Passed 300 volts
Latch-up	JESD78	Class II: Passed @ 85C Level A: Passed ± 200mA all pin

### LVC MOS DC Characteristics ( $V_{DD} = 2.97 - 3.63V$ , $T_A = -40^{\circ}C$ to $85^{\circ}C$ )

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V <sub>IH</sub>	Input HIGH voltage	2		$V_{DD} + 0.3$	V	3.3V Operation
V <sub>IL</sub>	Input LOW voltage	-0.3		0.8	V	3.3V Operation
V <sub>OH</sub>	Output HIGH voltage	2.37			V	$V_{DD} = 3.3V \pm 10\%$
V <sub>OL</sub>	Output LOW voltage			0.6	V	$V_{DD} = 3.3V \pm 10\%$

NOTE:

Output terminated with 50 Ohms to  $V_{DD}/2$ .

### LVDS DC Characteristics ( $V_{DD} = 2.97 - 3.63V$ , $T_A = -40^{\circ}C$ to $85^{\circ}C$ )

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V <sub>OH</sub>	Output HIGH voltage (Note 1)	1.248	1.375	1.602	V	
V <sub>OL</sub>	Output LOW voltage (Note 2)	0.898	1.025	1.252	V	
V <sub>OD</sub>	Output differential voltage	247	350	454	mV	
V <sub>CM</sub>	Common mode output voltage	1.125	1.2	1.375	V	

NOTE: Outputs terminated with 100 ohms between Q and  $\bar{Q}$ .

1.  $V_{OH\ max} = V_{CM\ max} + 1/2 V_{OD\ max}$

2.  $V_{OL\ min} = V_{CM\ min} - 1/2 V_{OD\ max}$

### LVPECL DC Characteristics ( $V_{DD} = 2.97 - 3.63V$ , $T_A = -40^{\circ}C$ to $85^{\circ}C$ )

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V <sub>OH</sub>	Output HIGH voltage	$V_{DD}-1.35$	$V_{DD}-1.01$	$V_{DD}-0.8$	V	
V <sub>OL</sub>	Output LOW voltage	$V_{DD}-2.0$	$V_{DD}-1.78$	$V_{DD}-1.6$	V	
V <sub>SWING</sub>	Peak to Peak Output Voltage Swing	0.65	0.77	0.95	V	

NOTE: Outputs terminated with 50 Ohms to  $V_{DD}-2$ .

### HCSL DC Characteristics ( $V_{DD} = 2.97 - 3.63V$ , $T_A = -40^{\circ}C$ to $85^{\circ}C$ )

Symbol	Condition	Min	Typ	Max	Unit
V <sub>OH</sub>	Output high voltage	660	700	850	mV
V <sub>OL</sub>	Output low voltage	-150	0		mV
V <sub>OVS</sub>	Max Output including Overshoot			$V_{OH} + 0.3$	V
V <sub>UDS</sub>	Min Output including Undershoot	$V_{OL} - 0.3$			V
V <sub>RB</sub>	Ringback Voltage	0.2			V
V <sub>OX</sub>	Absolute Crossing Point	250	450	550	mV
V <sub>swing</sub>	Peak to Peak Voltage Swing	650	700	950	mV

NOTE: Outputs terminated with 50  $\Omega$  to VSS

**LVCMOS AC Characteristics ( $V_{DD} = 2.97 - 3.63V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$ )**

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
FOUT	Output frequency	11.54		217.56	MHz	
TR / TF	Output rise/fall time	100		350	ps	20% to 80%
ODC	Output Duty Cycle	48	50	52	%	

**LVDS AC Characteristics ( $V_{DD} = 2.97 - 3.63V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$ )**

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
FOUT	Output frequency	11.54		217.56	MHz	
TR/TF	LVDS Output rise/fall time	85	140	350	ps	20% to 80%
ODC	Output Duty Cycle	48	50	52	%	

**LVPECL AC Characteristics ( $V_{DD} = 2.97 - 3.63V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$ )**

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
FOUT	Output frequency	11.54		217.56	MHz	
TR/TF	LVPECL Output rise/fall time	85	135	300	ps	20% to 80%
ODC	Output Duty Cycle	48	50	52	%	

**HCSL AC Characteristics ( $V_{DD} = 2.97 - 3.63V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$ )**

Symbol	Condition	Min	Typ	Max	Unit
TR/TF	Rise/Fall time	175	225	350	ps
ODC	Output Duty Cycle < 213 MHz	48	50	52	%
Fout	Output Frequency	11.54	217.56	217.56	MHz

## IC Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
VDD	Supply Voltage		2.97		3.63	V
IDD	Supply Current	LVPECL 217MHz			130	mA
IDD-OD	Supply Current - Output Disabled			68	88	mA
PSRR	Power Supply Rejection Ratio		-1.56	0.3	+1.56	ppm/V
PR	Pull Range		±100		±200	ppm
$K_{VCO}$	$V_C$ Transfer Function		66		167	ppm/V
T	Operating Temperature Range		-40		85	°C
Lin	Linearity	Note 2 - target ±2		±4		%
$T_{jit}$	Jitter	12 kHz - 20 MHz		0.25		ps-RMS
$F_{TSTAB}$	Frequency Temperature Stability	Note 3		±20		ppm
$F_{trimLSB}$	Frequency Trim Resolution (1 lsb)			0.5		ppm
$Z_C$	$V_C$ Input Impedance	$VDD = 3.3 \text{ 0} \leq V_C \leq VDD$	30	100		MΩ
$V_C$	$V_C$ Linear Input Range		0.3		2.7	V
$V_{c-trip}$	$V_C$ Trip point for Serial Interface		3.7	4.2	4.9	V
BW	Modulation Bandwidth	Note 1		25		kHz
ESD-MM	ESD tolerance, Machine Model		300			V
ESD-HBM	ESD tolerance, Human Body Model		3000			V

Note 1: IC is guaranteed to have > 30 kHz BW. Crystal measurements are needed to determine BW.

Note 2: Although linearity can be trimmed in OTP ROM, it also depends critically on crystal parameters.

Note 3: This is primarily a property of the crystal.

## Recommended Crystal Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
C0/C1	Crystal Pullability		210		280	
ESR	Equivalent Series Resistance				45	Ω
Freq	Crystal Frequency		20		40.6	MHz
C0	Crystal C0 Capacitance			2.0	4.0	pF

Note: Any crystal inharmonic tones must be 10dB or more below the fundamental mode.

Note: Crystal pull range depends on package parasitics, crystal Q, and C0.

For programming application notes describing programming details, contact the factory.

*Device information in register 0*

Manufacturer ID (11 bits) IEEE-1149.1 standard	Value= 0x0310 (Multigig JEDEC ID 16 in bank 7)
Product ID (8 bits)	Value=0x53
Product revision code (5 bits)	Value=0x02 (Revision 2)
Chip ID (7 bits)	Value normally 0x00 (unprogrammed)

Register 0: read only 32 bits

1	chip_id[6]	chip_id[5]	chip_id[4]	chip_id[3]	chip_id[2]	chip_id[1]	chip_id[0]	MSB
rev[4]	rev[3]	rev[2]	rev[1]	rev[0]	0	1	1	
0	0	0	1	0	0	0	0	
0	1	0	1	0	0	1	1	LSB

Register 3: read/write 24 bits PLL and output driver configuration

opdiv[7]	opdiv[6]	opdiv[5]	opdiv[4]	opdiv[3]	opdiv[2]	opdiv[1]	opdiv[0]	MSB
fbdiv[7]	fbdiv[6]	fbdiv[5]	fbdiv[4]	fbdiv[3]	fbdiv[2]	fbdiv[1]	fbdiv[0]	
VCOrange[2]	VCOrange[1]	VCOrange[0]	OT[1]	OT[0]	OEC[1]	OEC[0]	enbar_bypass	LSB

Register 5: read/write 16 bits Crystal parameters

NOT_USED	NOT_USED	freq_trim[5]	freq_trim[4]	freq_trim[3]	freq_trim[2]	freq_trim[1]	freq_trim[0]	MSB
gm_trim[3]	gm_trim[2]	gm_trim[1]	gm_trim[0]	NOT_USED	NOT_USED	NOT_USED	en_intrinsic	LSB

Chip\_id[6:0] may be read or programmed from the SPSP, but not written. Rev[4:0] records the chip revision and should read “2”.

Registers 1, 2, 4, 6, and 7 are for factory use - contact Multigig.

Linearity can be trimmed. Contact Multigig for more information.

En\_intrinsic enables a section of the linearization circuitry - leave 0 or consult Multigig.

freq\_trim[5:0] adds load capacitance in 31.7fF steps.

freq\_trim = 0, results in a 0pF load; freq\_trim = 63 results in a 2pF load.

gm\_trim[3:0] are encoded so that 1111 is the minimum, and 0000 is the maximum.

Opdiv and fbdiv produce undefined results if programmed below 16.

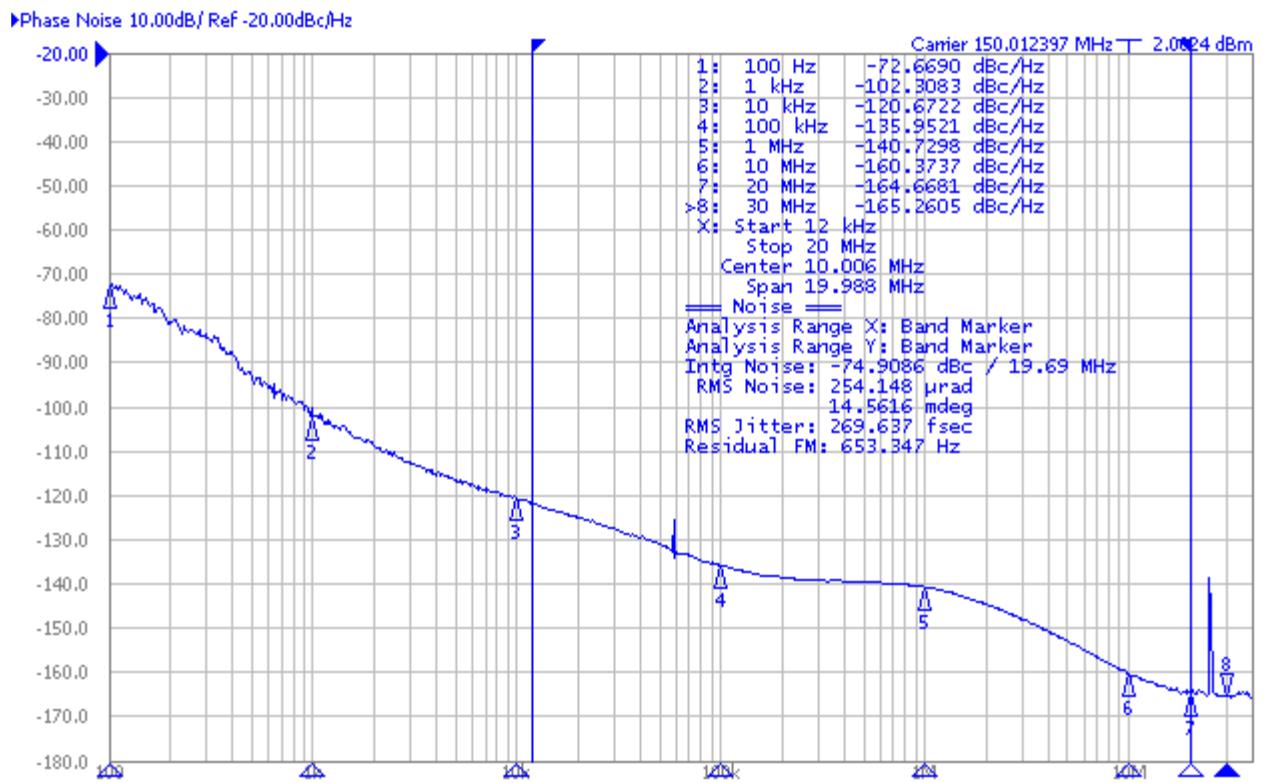
All bits are 0 in the unprogrammed state. Bits may be programmed incrementally, but no bit programmed to a “1” can be programmed to a “0.” Unused bits should be programmed to 0 to provide compatibility with future product enhancements.

### Crystal Freq vs Default gm Setting

Crystal Freq	Default gm_trim
<25MHz	13
30MHz	12
35MHz	10
38MHz	9
40MHz	8
Higher ESR crystals and/or higher C <sub>L</sub> may require higher gm_trim settings (lower numeric value).	

rev[4:0]	Part Revision
1	A engineering
2	B first production

A bypass feature is added in revision B that buffers the crystal frequency to the Q output in CMOS mode until enbar\_bypass is programmed to 1. The unprogrammed part will bypass the PLL for crystal frequency trimming.



Typical Phase Noise: 25.0MHz crystal, 150.0 MHz output,  $V_c=1.5V$

## Example register values for some common frequencies

Crystal Frequency	Output Frequency	VCOrange [2:0] Register 3 [7:5]	fbdiv [7:0] Register 3 [15:8]	opdiv [7:0] Register 3 [23:16]
30.65 - 31.98	122.58 - 127.92	100	96 = 0x60	24 = 0x18
24.63 - 25.80	123.51 - 129.00	001	130 = 0x82	26 = 0x1a
38.12 - 39.93	152.48 - 159.71	001	84 = 0x54	21 = 0x15
32.02 - 33.54	160.10 - 167.70	001	100 = 0x64	20 = 0x14
33.21 - 34.81	166.05 - 174.05	000	100 = 0x64	20 = 0x14
33.35 - 34.94	200.14 - 209.65	001	96 = 0x60	16 = 0x10
34.59 - 36.26	207.65 - 217.56	000	96 = 0x60	16 = 0x10

The table above is an example only. Any frequency can be supported as long as the following 3 equations are met:

Output frequency X opdiv = VCO frequency

VCO frequency = Crystal frequency x fbdiv

2942 MHz ≤ VCO frequency ≤ 3481 MHz

<h3>LVPECL test circuit</h3> <p>Vdd power Vdd = 2.0V</p> <p>Vss power = -1.3V</p> <p>Leave Vdd fixed at 2.0V and adjust Vss.</p>	<h3>LVDS test circuit</h3> <p>Vdd power Vdd = 2.1V</p> <p>Vss power = -1.2V</p> <p>Leave Vss fixed at -1.2V and adjust Vdd.</p>
<h3>LVC MOS test circuit</h3> <p>Vdd power Vdd = 1.65V</p> <p>Vss power = -1.65V</p> <p>Adjust Vss and Vdd together.</p>	<h3>HCSL test circuit</h3> <p>Vdd power Vdd = 3.3V</p> <p>Adjust Vdd.</p>
<p>All equipment is 50Ω to ground. All cables are 50Ω.  Vc and OE should be set to voltages appropriate to the test; do not float Vc.  Industry standard package top-view shown.  LVDS and LVC MOS tests may optionally be C-coupled. LVPECL and HCSL require the DC bias shown.</p>	

## Ordering Information

Order Number	Top Marking	Package	Shipping	Temperature
MQC203BD-Y		Die	Trays	-40°C to 85°C

Devices are Green, RoHS Compliant and PFOS Compliant.

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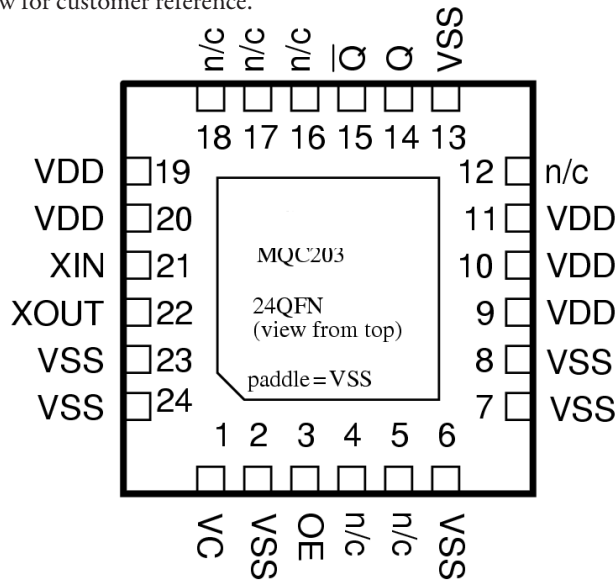
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The MQC203 has been sampled in 24-pin QFN packages for customer evaluation. The package is shown below for customer reference.



24-pin QFN. 4 mm x 4 mm package, 0.5 mm pitch  
 Note: All VDD and VSS are common on the IC.

### Revision History Sheet

Silicon Rev	Datasheet Rev	Page	Date	Description of Change
A	0.991		09/09/10	Initial Engineering Preliminary Information
A	0.992	5,6	09/10/10	Removed non-customer registers. Added bit definitions. Added HCSL to title
A	0.993	6	09/10/10	Rev change only
A	0.994	6	09/17/10	OEC[1:0] table error. Minor cosmetic changes
A	0.995	1	09/21/01	New OEC table and explanation. Block diagram R=50k
A	0.997	9,10	01/19/10	Added bypass mode. Updated revision codes. Added Revision History
B	0.998	6,7,8	02/24/11	Added Fout min/max for all outputs. Changed Crystal C0/C1 min/max, added crystal note. Changed definition of Gm_trim, and added bypass feature.
B	0.999	8,10	3/16/11	Default gm_trim table corrected. Example register; register number and bits corrected
B	0.991	11	05/31/11	Added test circuit, page 11
B	1.00			Initial Production Datasheet