

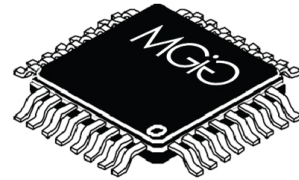
Clock Synthesizer 50-800 MHz LVPECL

Product Description

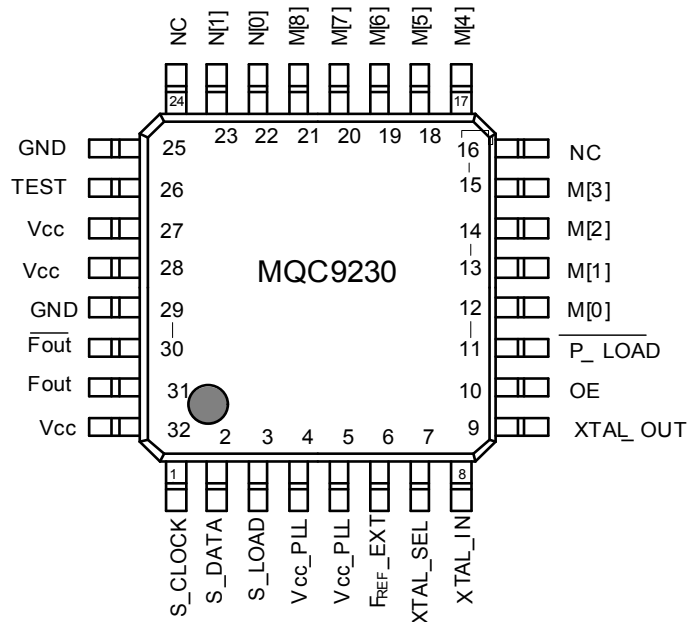
The MQC9230 is part of the QuietClock™ series from Multigig, providing a near ideal clock signal for QDR and SDR Memories from 50MHz to 800MHz. The MQC9230 utilizes an integrated crystal oscillator and an external crystal to generate an internal reference signal which is subsequently multiplied by the PLL and scaled by an output divider to generate output frequencies from 50 to 800 MHz. Programmability is provided both via a 3 wire Serial Interface and full access to the M (9 bits) & N (2 bits) divider settings via external pins. Very low jitter and the use of high performance LVPECL output buffers makes the MQC9230 ideal for mid-range to high-performance applications in telecom and networking.

Features

- LVC MOS compatible control inputs
- Integrated loop filter components
- Integrated reference oscillator
- Input crystal frequency: 10 - 20 MHz
- Output frequency: 50 - 800 MHz, selectable
- Extremely low jitter: < 25ps cycle-cycle RMS
- Low power consumption: 47mA no-load
- 3.3 Volt operation
- Selectable external reference
- LVPECL outputs 25ohm capable
- Available in 32-Lead Green TQFP
- Industrial grade is standard (-40 to 85°C)
- Test mode providing performance verification
- Pin compatible with Motorola/Freescale & IDT IDT/MPC9230

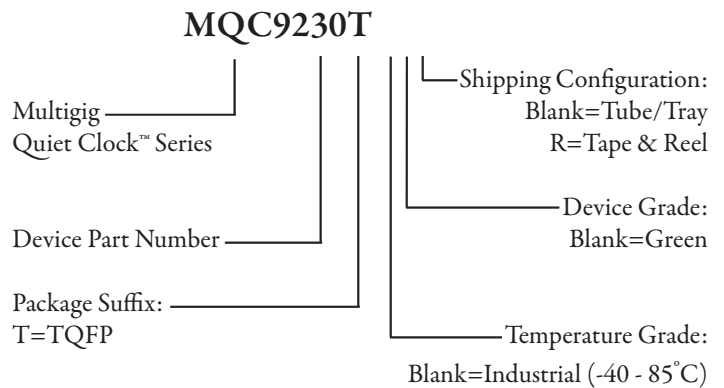


32-Lead TQFP



MQC9230 32-Lead TQFP Pinout
(Top View)

MQC9230 Part Number:



MQC9230 Block Diagram

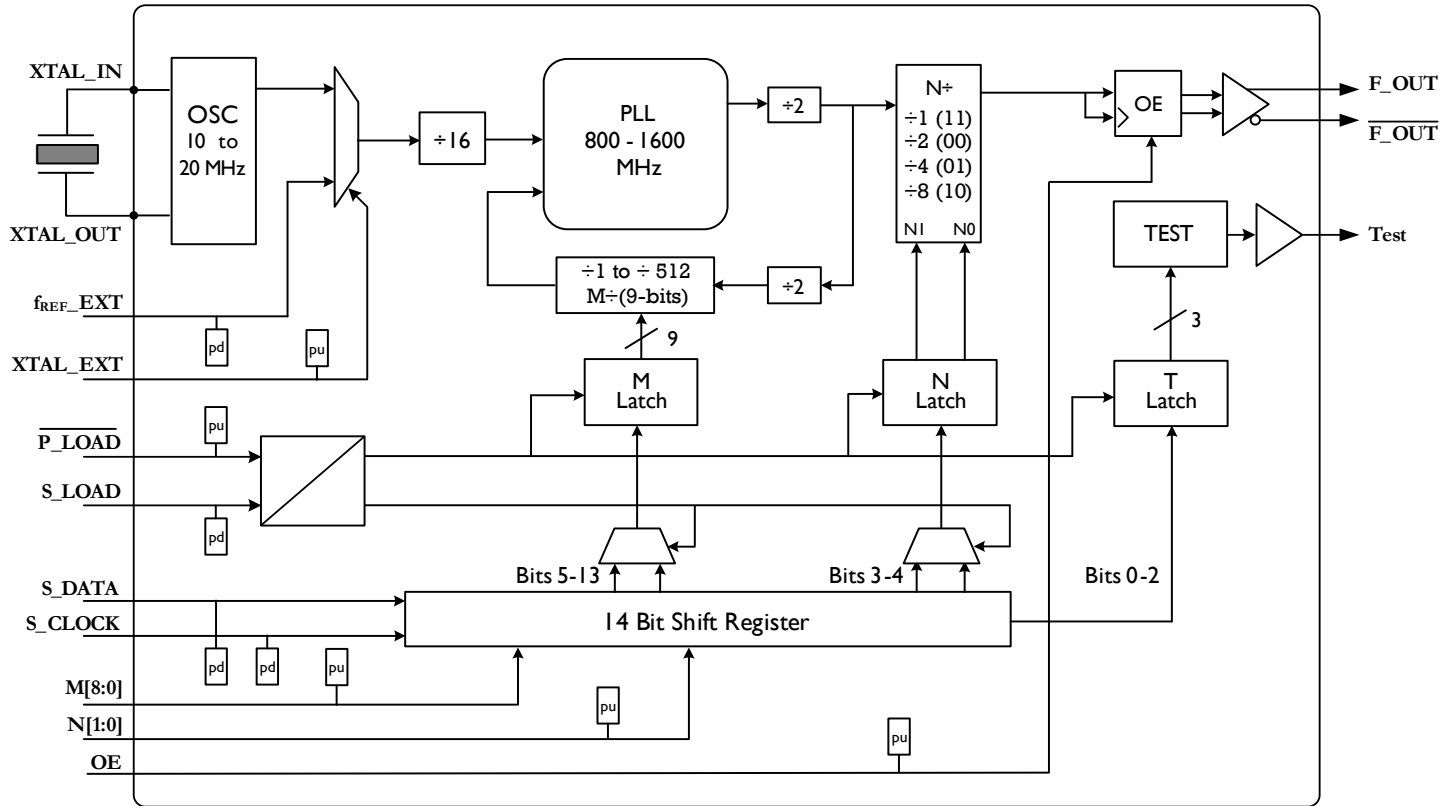


Figure-1

Device Description

The internal crystal oscillator requires an external quartz crystal to function as a reference oscillator. Referring to figure 1 above, the frequency of the internal oscillator is divided by 16 and subsequently multiplied by the PLL to achieve the desired output frequency. The crystal oscillator reference signal 'Fxtal', the PLL feedback divider 'M' and the PLL post-divider 'N' together determine the output frequency. The PLL feedback 'M' value is programmed via the serial or parallel interface. The PLL post divider 'N', is also programmed via the serial or parallel interface. Once programmed, the internal PLL adjusts the RotaryWave™ VCO output frequency to effectively be 'M' times the divided reference frequency by adjusting the RotaryWave™ VCO input control voltage. As shown figure 1, the PLL post divider 'N' divides by 1, 2, 4, or 8, while the PLL feedback divider 'M' values range from 1-512. The configuration logic has 2 sections – serial & parallel. The parallel interface uses the values at M [8:0] & N [1:0] to configure the counters. The serial interface contains a 14-bit shift register, which shifts once per rising edge of the S_CLOCK input. The internal PLL is always guaranteed to be stable when the RotaryWave™ VCO is operated within its specified range.

The MQC9230's output is derived differentially from the PLL post divider 'N' output and supports driving dual 50Ω transmission lines to $V_{CC} - 2.0V$. To minimize noise induced jitter, the power source for the output driver is isolated from the core and PLL power. Upon reset/power-up it is recommended to hold the P_LOAD input LOW until power is stable. The TEST function allows inspection of various internal nodes and is controlled via the T [2:0] bits in the serial data stream. For other packaging options, or 2.5 volt operation, please contact Multigig.

IC Pinout Description

Pin #	Name	Type	Level	Description
1	S_CLOCK	In	pulldown	Serial configuration clock.
2	S_DATA	In	pulldown	Serial configuration data.
3	S_LOAD	In	pulldown	Serial configuration control input. This is a transparent latch.
4	V _{CC_PLL}	Pwr		Positive power supply for PLL.
5	V _{CC_PLL}	Pwr		Positive power supply for PLL.
6	F _{REF_EXT}	In	pulldown	Alternative PLL reference input.
7	XTAL_SEL	In	pullup	PLL reference input select.
8	XTAL_IN	In		Crystal oscillator input.
9	XTAL_OUT	In		Crystal oscillator output.
10	OE	In	pullup	Output enable. Active high.
11	$\overline{P_LOAD}$	In	pullup	Parallel configuration control input. This is a transparent latch.
12	M[0]	In	pullup	Parallel configuration data for divider M.
13	M[1]	In	pullup	Parallel configuration data for divider M.
14	M[2]	In	pullup	Parallel configuration data for divider M.
15	M[3]	In	pullup	Parallel configuration data for divider M.
16	NC			
17	M[4]	In	pullup	Parallel configuration data for divider M.
18	M[5]	In	pullup	Parallel configuration data for divider M.
19	M[6]	In	pullup	Parallel configuration data for divider M.
20	M[7]	In	pullup	Parallel configuration data for divider M.
21	M[8]	In	pullup	Parallel configuration data for divider M.
22	N[0]	In	pullup	Parallel configuration data for divider N.
23	N[1]	In	pullup	Parallel configuration data for divider N.
24	NC			
25	GND	Pwr		Ground.
26	TEST	Out		Test and device diagnosis output.
27	V _{CC}	Pwr		Power supply for I/O and core.
28	V _{CC}	Pwr		Power supply for I/O and core.
29	GND	Pwr		Ground.
30	$\overline{F_{OUT}}$	Out		Differential output clock.
31	F _{OUT}	Out		Differential output clock.
32	V _{CC}	Pwr		Power supply for I/O and core.

Input capacitance = 4 pF typical, All termination (pullup / pulldown) resistors are 75kΩ.

General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC}-2$		V	
MM	ESD Protection (machine model)	200			V	
HBM-RF	ESD Protection (human body model) ($F_{OUT}, \overline{F_{OUT}}$)	2000			V	
HBM	All others	4000			V	
LU	Latch-Up Immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs

Absolute Maximum Ratings

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	4.6	V	
V_{IN}	DC Input Voltage	-0.3	$V_{CC}+0.3$	V	
V_{OUT}	DC Output Voltage	-0.3	$V_{CC}+0.3$	V	
I_{IN}	DC Input Current		+/-20	mA	
I_{OUT}	DC Output Current		+/-50	mA	
T_S	Storage Temperature	-65	125	°C	

DC Characteristics ($V_{CC} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS Control Inputs (F_{REF} -EXT, XTAL_SEL, $\overline{P_LOAD}$, S_LOAD, S_CLOCK, M[0:8], N[0:1], OE)						
V_{IH}	Input High Voltage	2.0		$V_{CC}+0.3$	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
I_{IN}	Input Current			+/-200	μA	$V_{IN} = V_{CC}$ or GND
Differential Clock Output F_{OUT} (See Note-1)						
V_{OH}	Output Voltage High	$V_{CC}-1.037$	$V_{CC}-0.960$	$V_{CC}-0.871$	V	LVPECL †
V_{OL}	Output Voltage Low	$V_{CC}-1.888$	$V_{CC}-1.750$	$V_{CC}-1.577$	V	LVPECL †
TEST Output						
V_{OH}	Output Voltage High	2.0		$V_{CC} + 0.3$	V	$I_{OH} = -0.80$ mA
V_{OL}	Output Voltage Low			0.5	V	$I_{OL} = 0.80$ mA
Supply Current						
I_{CC_PLL}	PLL Supply Current		4	10	mA	V_{CC_PLL} Pins
I_{CC}	Supply Current (no load)		50	58	mA	All V_{CC} Pins

† Note-1: F_{OUT} and $\overline{F_{OUT}}$ terminated with 50 Ω to $V_{CC}-2.0$ Volts.

AC Characteristics ($V_{CC} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
F_{XTAL}	Crystal Frequency Range	10		20	MHz	
F_{REF}	F_{REF_EXT} Frequency Range	10		20	MHz	
F_{VCO}	VCO Frequency Range	800		1600	MHz	
F_{MAX}	Output Frequency	400		800	MHz	N1:N0 N = 11 ($\div 1$)
		200		400	MHz	N = 00 ($\div 2$)
		100		200	MHz	N = 01 ($\div 4$)
		50		100	MHz	N = 10 ($\div 8$)
F_{S_CLOCK}	Serial Programming Clock	0		25	MHz	
t_{P_MIN}	Minimum Pulse Width	50			ns	
$t_{P_P_Load}$ $t_{P_S_Load}$	Minimum Latch Pulse Width	50			ns	
DC	Output Duty Cycle	48	50	52	%	50MHz-400MHz
		46.5	50	53.5		400MHz-800MHz
t_r, t_f	Output Rise / Fall Time †	114	180	239	ps	20% to 80%
t_s	Setup Time	20			ns	S_DATA to CLOCK
		20			ns	CLOCK to S_DATA
		20			ns	M, N to $\overline{P_LOAD}$
t_h	Hold Time	20			ns	S_DATA to CLOCK
		20			ns	M, N to $\overline{P_LOAD}$
$t_{JIT(CC)}$	Cycle - Cycle Jitter RMS Filter as per page 9		12	22	ps	N = 11 ($\div 1$)
			15	23	ps	N = 00 ($\div 2$)
			17	27	ps	N = 01 ($\div 4$)
			20	37	ps	N = 10 ($\div 8$)
$t_{JIT(PER)}$	Period Jitter RMS Filter as per page 9		7	14	ps	N = 11 ($\div 1$)
			8	16	ps	N = 00 ($\div 2$)
			10	18	ps	N = 01 ($\div 4$)
			12	24	ps	N = 10 ($\div 8$)
t_{LOCK}	PLL Lock Time		0.75	10	ms	
t_{stable}	Output clock stable after power-up		0.75	10	ms	

† Not applicable to TEST Output

 Note: AC Characteristics apply for F_{OUT} and $\overline{F_{OUT}}$ terminated with 50Ω to $V_{CC}-2.0$ Volts.

MQC9230 Frequency Operating Range (MHz)

M	M[8:0]	PLL frequency given a Xtal frequency of:						Output frequency: Xtal = 16 MHz			
		10MHz	12MHz	14MHz	16MHz	18MHz	20MHz	N: ÷ 1	N: ÷ 2	N: ÷ 4	N: ÷ 8
160	010100000						800				
170	010101010						850				
180	010110100					810	900				
190	010111110					855	950				
200	011001000				800	900	1000	400	200	100	50
210	011010010				840	945	1050	420	210	105	52.5
220	011011100				880	990	1100	440	220	110	55
230	011100110			805	920	1035	1150	460	230	115	57.5
240	011110000			840	960	1080	1200	480	240	120	60
250	011111010			875	1000	1125	1250	500	250	125	62.5
260	100000100			910	1040	1170	1300	520	260	130	65
270	100001110		810	945	1080	1215	1350	540	270	135	67.5
280	100011000		840	980	1120	1260	1400	560	280	140	70
290	100100010		870	1015	1160	1305	1450	580	290	145	72.5
300	100101100		900	1050	1200	1350	1500	600	300	150	75
310	100110110		930	1085	1240	1395	1550	620	310	155	77.5
320	101000000	800	960	1120	1280	1440	1600	640	320	160	80
330	101001010	825	990	1155	1320	1485		660	330	165	82.5
340	101010100	850	1020	1190	1360	1530		680	340	170	85
350	101011110	875	1050	1225	1400	1575		700	350	175	87.5
360	101101000	900	1080	1260	1440			720	360	180	90
370	101110010	925	1110	1295	1480			740	370	185	92.5
380	101111100	950	1040	1330	1520			760	380	190	95
390	110000110	975	1070	1365	1560			780	390	195	97.5
400	110010000	1000	1200	1400	1600			800	400	200	100
410	110011010	1025	1230	1435							
420	110100100	1050	1260	1470							
430	110101110	1075	1290	1505							
440	110111000	1100	1320	1540							
450	111000010	1125	1350	1575							

Output Frequency Range and PLL Post-Divider N

N		VCO Output Frequency Division	F _{OUT} Frequency Range -40°C to 85°C
1	0		
0	0	1	200 – 400 MHz
0	1	2	100 – 200 MHz
1	0	4	50 – 100 MHz
1	1	8	25 – 50 MHz

Programming the MQC9230

Programming and configuring the MQC9230 to produce the desired output frequency can be represented by the following formulas:

- (1) $F_{OUT} = (F_{XTAL} \div 16) * (4 * M) \div (2 * N)$ or;
- (2) $F_{OUT} = (F_{XTAL} \div 8) * (M \div N)$

where F_{XTAL} is the XTAL Frequency, 'M' is the PLL feedback divider, and 'N' is the PLL post-divider. The input Frequency and the selection of the feedback divider 'M' is limited by the VCO frequency range. F_{XTAL} and 'M' must be configured to match the VCO frequency range of 800 to 1600 MHz in order to achieve stable PLL operation.

- (3) $M_{MIN} = 4 * F_{VCO.MIN} \div F_{XTAL}$ and;
- (4) $M_{MAX} = 4 * F_{VCO.MAX} \div F_{XTAL}$

As an example, using a 16 MHz input frequency requires the configuration of the PLL feedback divider 'M' between 200 and 400. The following table shows the usable VCO frequency and 'M' divider ranges. Assuming a 16 MHz input, the equation reduces to:

- (5) $F_{OUT} = 2 * M \div N$

Substituting 'N' with the four available values for 'N' (1, 2, 4, 8) yields output frequencies in MHz.

Function Table

Input	0	1
XTAL_SEL	F _{REF_EXT}	XTAL interface
OE	Outputs disabled (F _{OUT} =0, F _{OUT} =1)	Outputs enabled

Output Frequency Range for 16 MHz Crystal

N			F _{OUT}	F _{OUT} Range MHz	F _{OUT} Step MHz
1	0	Value			
0	0	2	M	200 - 400	1
0	1	4	M ÷ 2	100 - 200	0.5
1	0	8	M ÷ 4	50 - 100	0.25
1	1	1	M * 2	400 - 800	2

Example using a 16 MHz Crystal Frequency

If an output frequency of 131 MHz was desired, the following steps would be taken to identify the appropriate 'M' & 'N' values. Based upon the table above, 131 MHz falls in the frequency range set by an 'N' value of 4, so N[1:0]=01. For N = 4, the output frequency is: $F_{OUT} = M \div 2$ and $M = F_{OUT} * 2$. Therefore $M = 2 * 131 = 262$, so M[8:0] = 100000110. Following this procedure the designer can generate any whole frequency between 50 MHz and 800 MHz. The size of the programmable frequency steps will be equal to: $f_{STEP} = f_{XTAL} \div 8 \div N$

Crystal Specifications Overview

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance
Frequency Tolerance	+/-75 ppm at 25°C
Frequency/Temperature Stability	+/-150 ppm at 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5-7pF
Equivalent Series Resistance (ESR)	50 to 80 Ω
Correlation Drive Level	100 μW

Using TEST Diagnostics and Output

The TEST output provides added visibility for one of the several internal critical nodes as determined by the T [2:0] bits in the serial configuration data stream. This should be used for Test purposes ONLY, and it is not recommended to select the F_{OUT} signal through this CMOS output. The ‘T’ Bits are preset to 000 when P_LOAD is LOW so the LVPECL outputs are as free of noise as is possible. Any active signal on the TEST output will adversely affect the jitter performance of the LVPECL output pair. The TEST pin must be static for normal operation to guarantee the jitter specifications. Most of the signals available on the TEST output pin are useful only for performance verification of the MQC9230. The PLL Bypass mode can be selected when T[2:0] is set to 110. In this mode the S_CLOCK input is fed directly into the M & N dividers. The N divider drives the F_{OUT} differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input can be used for low speed PCB debug or functional testing. Bypassing the PLL and driving the F_{OUT} directly gives the user more control of the test clocks sent through the clock tree and shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level the input frequency is limited to 200 MHz. This means the fastest the Fout pin can be toggled reliably via S_CLOCK is 200MHz, when the divider ratio of the post-PLL divider is 1 (N=3). The M counter output of the TEST output may not (it will be 50 or near 50) be equal to 50% duty cycle.

Test and Diagnostics Setup

T[2:0]			TEST Output
T2	T1	T0	
0	0	0	14-bit shift register out
0	0	1	Logic 1
0	1	0	F _{XTAL} ÷ 16
0	1	1	M-Counter output
1	0	0	F _{OUT}
1	0	1	Logic 0
1	1	0	M-Counter Bypass Mode
1	1	1	F _{OUT} ÷ 4

Debug Configuration for PLL Bypass

Output	Configuration
F _{OUT}	S_CLOCK ÷ N
TEST	S_CLOCK ÷ 2M

Notes: T[2:0] = 110
AC specifications do not apply in PLL bypass mode.

Serial and Parallel Interfaces

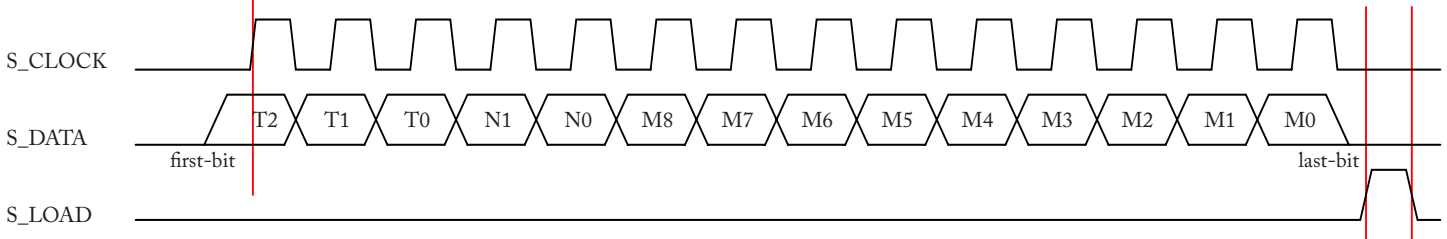
The ‘M’ & ‘N’ counters can be loaded either thru a parallel or serial interface. When the P_LOAD signal is LOW, the input latches will become transparent, thus any changes on ‘M’ or ‘N’ inputs will affect the F_{OUT} output pair. When utilizing the serial port, the S_CLOCK signal samples the information on the S_DATA line and loads it into a 14 Bit shift register. The P_LOAD signal must be HIGH for the serial operation to function. The TEST register is loaded with the first 3-Bits, the ‘N’ register with the next 2, and the ‘M’ register with the final 9-bits of the data stream on S_DATA. For each register, the most significant bit is loaded first (T2, N1 and M8). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters.

Serial & Parallel Timing Diagram

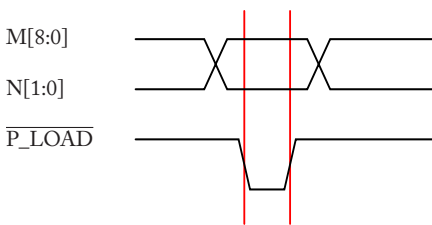
The timing diagram for both serial and parallel loading scenarios is shown on the following page. Referring to the diagram; M[8:0] and N[1:0] are normally specified at power-up post reset via the parallel interface. Subsequent to the parallel load, the serial interface can be utilized to change and fine tune the output frequency. This sequence allows the synthesizer to come up at one frequency while adding the flexibility of serial programming.

Serial & Parallel Interface Timing Diagram

Serial Interface Timing



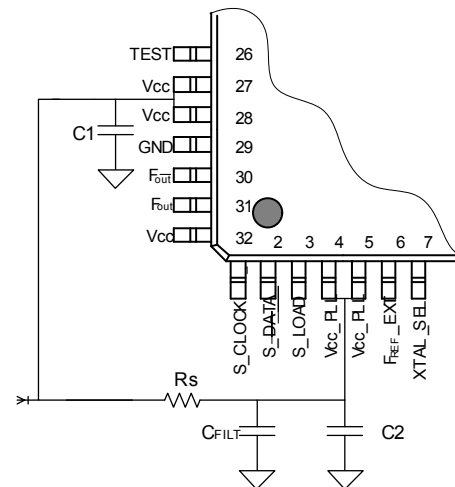
Parallel Interface Timing



S_LOAD is an active high transparent latch. $\overline{P_LOAD}$ is an active low transparent latch. Data should not change while these signals are active. In the simplest case, for a fixed value of M and N, $\overline{P_LOAD}$ may be tied to ground, in which case M and N are loaded on an internal power-on reset signal. A parallel load always sets the internal T register to zero.

Power Supply Filtering Suggestions

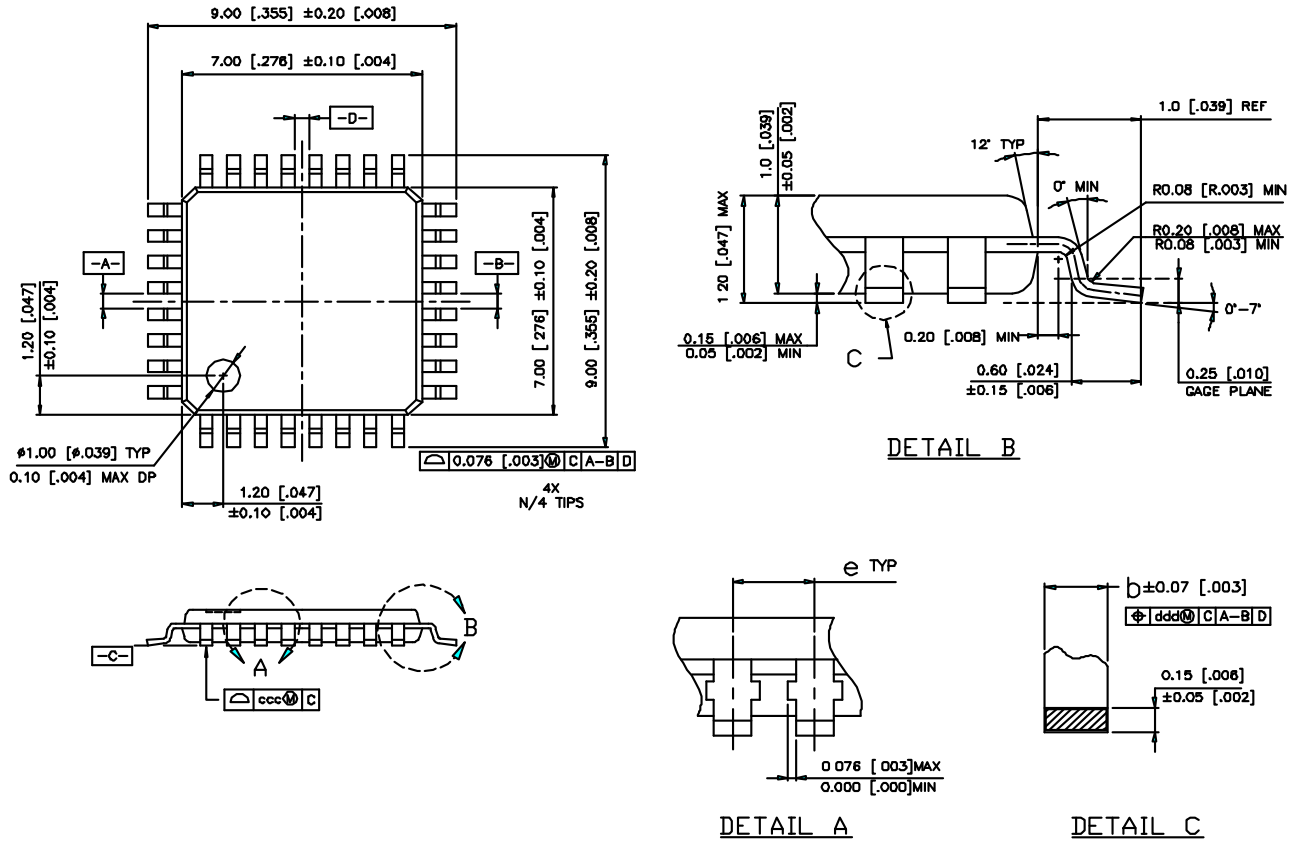
The MQC9230 is a mixed analog/digital product. Its analog circuitry is susceptible to random noise, especially noise on the power supply pins. Random noise on the V_{CC_PLL} pin significantly affects the device performance. The MQC9230 provides separate power supplies for the digital (V_{CC}) and the internal PLL (V_{CC_PLL}) of the device. The purpose of this design technique is to isolate the switching noise of the digital outputs from the sensitive analog PLL. The simplest form of isolation is a power supply filter on the V_{CC_PLL} pin. The figure to the right illustrates a typical power supply filtering method. The RC filter will provide a broadband filter with a 100:1 attenuation for noise in the spectral content above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor RLC-model, the net reactance becomes purely inductive, thus the reactance increases with frequency above this point. Adding a second parallel capacitance C2, with an increased series resonance alleviates this problem. The capacitors should be carefully selected to provide a low impedance path to ground for frequencies significantly above the PLL bandwidth. Manufacturers data sheets should be consulted when selecting any surface mount capacitor to insure the series resonance of the capacitor is not exceeded well above the highest frequency of concern. Additional attenuation can be achieved by placing an inductor in series with the resistor.



Typical Filter Values

$C1 = C2 = 0.01$ to $0.10 \mu\text{F}$
 $C_{\text{FILT}} = 22 \mu\text{F}$
 $R_s = 240\Omega$

Package Outline Drawing



Notes:

1. Drawing conforms to JEDEC ref. MS-026 rev. C.
2. Controlling dimensions in mm.
3. Pin-1 indicator may be corner chamfer, dot or both.
4. Center line reference is defined by the midpoint of the center lead or the center space between leads at the package.

Variations:

Lead Count	e	b			ccc	ddd
		MIN	NOM	MAX		
32L	0.80 mm	0.300 mm	0.370 mm	0.450 mm	0.100 mm	0.200 mm
	0.031 in	0.012 in	0.015 in	0.018 in	0.004 in	0.008 in

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