

25.5 Multi-Gigahertz Low-Power, Low-Skew, Rotary Clock Scheme

John Wood¹, Steve Lipa², Paul Franzon², Michael Steer²

¹Multigig Corporation Ltd.

²North Carolina State University

On-chip clock frequencies in the gigahertz range require generators with low skew and low jitter in order to avoid timing problems. Traditional approaches to the clock distribution problem start to become untenable in the gigahertz range. For example, H-trees require careful balancing and are difficult to implement for multi-gigahertz operation even for submicron CMOS processes. Other systems, such as salphasic distribution [1] and distributed amplifiers [2] provide a sinusoidal clock, making fast edge rates difficult to achieve. In this paper we describe a rotary clock distribution architecture which provides low-skew, low-jitter, gigahertz-rate clocking with high edge rates and low power consumption, works over a wide power supply range and is completely scalable. The frequency is only limited by the f_t of the integrated circuit technology used; an f_t of approximately 30 GHz produces square waves with 20 ps transition times. In addition, there is no limit to the size of the chip that can be clocked, and both multiphase and non-overlapping noise immune differential clocking are supported.

The basic architecture is shown in Fig. 1. This is a layout of a 2.5 GHz rotary clock with 25 interconnected rings. Each ring consists of a differential line driven by shunt connected anti-parallel inverters which are distributed around the ring. This arrangement produces a clock wave that rotates around the ring at a rate that depends primarily on the electrical length of the ring. Rotation is locked and amplitude is maintained by the switching transistors in spite of conductor losses.

Unlike a ring oscillator, the energy that goes into charging and discharging inverter inputs becomes transmission line energy which is recirculated in the closed electromagnetic path, providing a significant power savings as losses are due only to I^2R dissipation in the wires and not CV^2f related dissipation. The power savings are further enhanced when copper metalization is used.

Fig. 2 illustrates the theory behind the rotary clock architecture. Fig. 2a shows an open loop of differential conductors connected to a battery through an ideal switch. When the switch is closed, a voltage wave begins to travel counterclockwise around the loop. Fig. 2b shows a similar loop, with the voltage source replaced by a cross-connection of the inner and outer conductors. If there are no losses, a wave travelling on this ring will continue indefinitely, providing a full clock cycle every other round trip of the edge. The inversion occurs at the crossover. In order to overcome losses and provide a startup signal, at least one anti-parallel inverter pair is required. Power supply ramp up or any other noise event will initiate startup of the rotary wave. Once the wave is established it takes very little power to sustain it. Also, since there are exactly 180 degrees of phase shift for each rotation around the ring, the relative phase and therefore clock skew at any point on the ring is well known.

Interconnected rings, as in Fig. 1a, must run in lock step. This ensures that the same signal appears on each ring and that the relative phase at all points on all the rings is well known. Thus by choosing the correct pick-off point on each ring it is possible to use a large array of interconnected rings to distribute a clock signal over an arbitrarily large die area with minimal clock skew. For example, referring to Fig. 1a, all the points marked with the equals sign (=) have the same relative phase. By choosing a pick-off point that is diametrically opposite to a given pick-off point, it is possible to obtain the opposite

phase, and in principle an arbitrary number of phases can be extracted.

The rotary clock is modeled as short lengths of transmission line between inverter pairs which present substantial capacitive loading. Fig. 3a shows the transmission line model consisting of the $L_{line}/2$ inductance and the $C_{line, AB}$ line-to-line capacitance surrounding the inverters. Fig. 3b shows the full model of the transmission line element with all of the transistor capacitances broken out. Given that L and C are the inductance and capacitance per unit length of the differential line, C_i is the total input capacitance of each inverter, and that there are N inverters per unit length around the ring, the effective parameters describing the loaded ring are: $L_{eff} = L$; $C_{eff} = C + 0.5 * C_i * N$; $Z_{0eff} = \text{root}(L_{eff}/C_{eff})$; $v_p = 1/\text{root}(L_{eff} * C_{eff})$.

Clock frequency is approximately $f_c = v_p/(2 * l)$ where l is the length of the ring. Nominal clock frequency is selected by varying L_{eff} and C_{eff} , which can be accomplished by meandering the lines and by adding gate-channel capacitances along the lines.

Fig. 4 shows a die photograph of a prototype built using a 0.25 μm 2.5 V CMOS process with 1 μm AlCu. The prototype features a large ring which is completely independent of five interconnected smaller rings. The 12000 μm outer ring uses 60 μm conductors on a 120 μm pitch, with 128 62.5 $\mu\text{m}/25 \mu\text{m}$ inverter pairs distributed along its length. Interconnect segments were modeled using a 20 pole equivalent LR matrix generated using FASTHENRY [3]. Inverters were modeled using BSIM3v3 non-quasi-static transistor models. Simulations predicted a clock frequency of approximately 925 MHz. Measurements of the actual performance of the large ring with $V_{ss} = 2.5$ V vs. simulation results are shown in Fig. 5. The oscillation frequency was 965 MHz. Jitter was measured at 5.5 ps RMS using a Tektronix 11801A oscilloscope with an SD-26 sampling head. Fig. 6 shows that the oscillation frequency is quite flat over a large V_{dd} range and that total chip power consumption is quite low. Clock generator simultaneous switching transients are eliminated by the distributed switching times of each inverter, allowing operation with just 15 pF of on-chip capacitance and no off-chip decoupling while driving multiple 10 Ω impedance lines. Fig. 7 shows the measured waveform on one of the smaller rings, which has not yet been fully characterized. Oscillation frequency is 3.38 GHz vs. a simulated frequency of 3.42 GHz.

Acknowledgements:

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References:

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- [2] Bendik Kleveland *et al.*, "Monolithic CMOS Distributed Amplifier and Oscillator," ISSCC Digest of Technical Papers, 1999, pp. 70-71.
- [3] Kamon, M. *et al.*, "FASTHENRY: a multipole-accelerated 3-D inductance extraction program," IEEE Trans. Microwave Theory and Techniques, Vol 42, Sept. 1994, pp. 1750-1758.

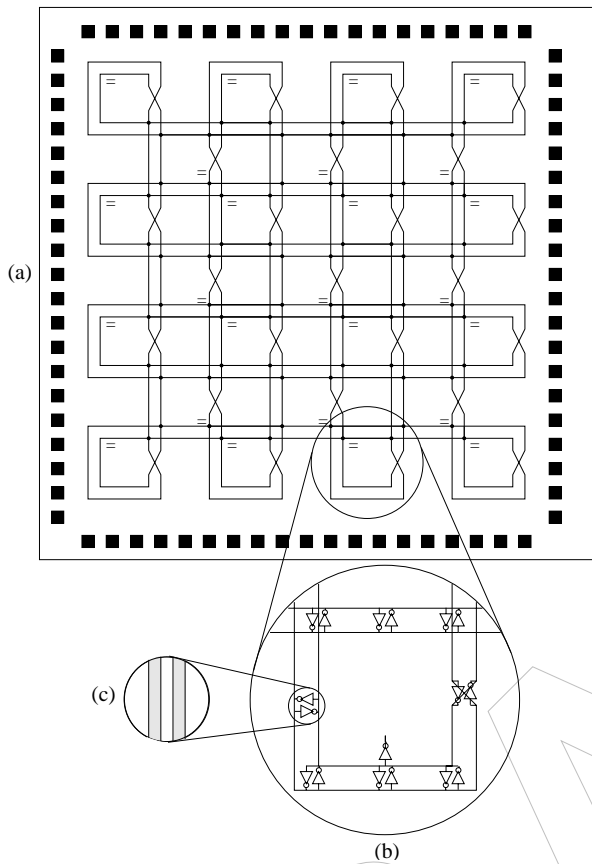


Figure 1) Basic rotary clock architecture. The = signs denote points with equivalent phase.

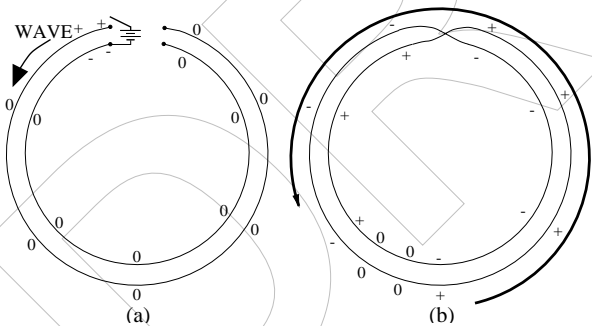


Figure 2) Genesis of the wave on the ring.

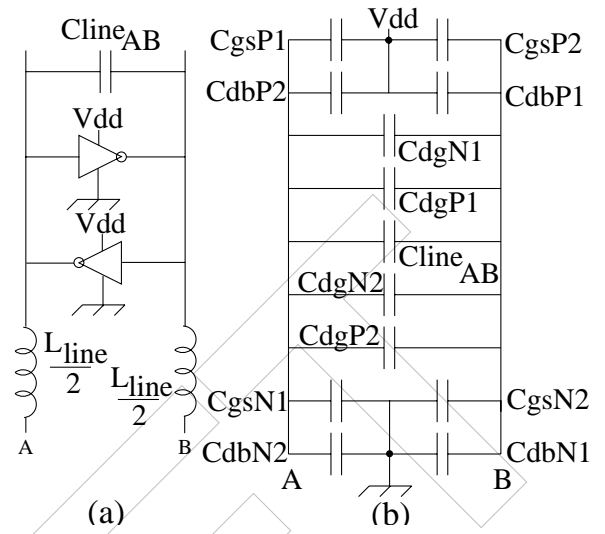


Figure 3) Development of the rotary clock model. (a) shows the macromodel of a transmission line segment. (b) shows capacitances of the transistors broken out.

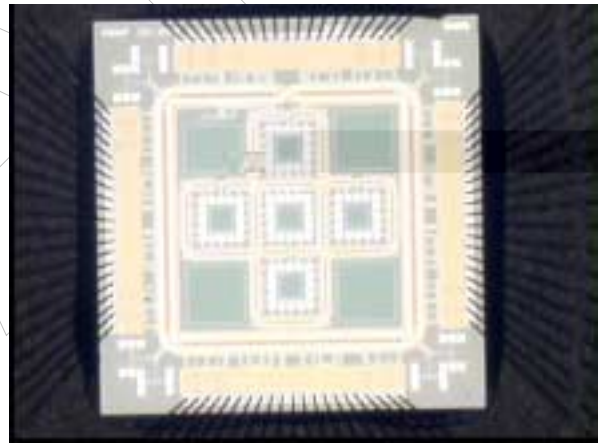


Figure 4) Die photograph of prototype chip.

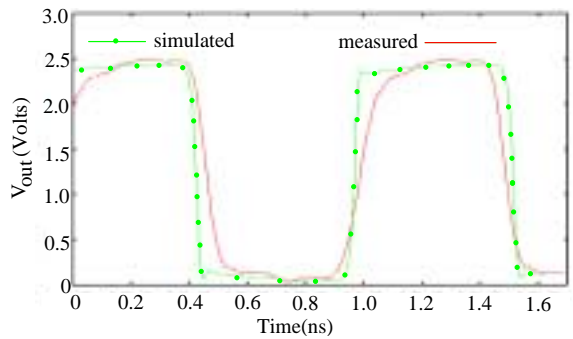


Figure 5) Measurement vs. simulation for large ring.

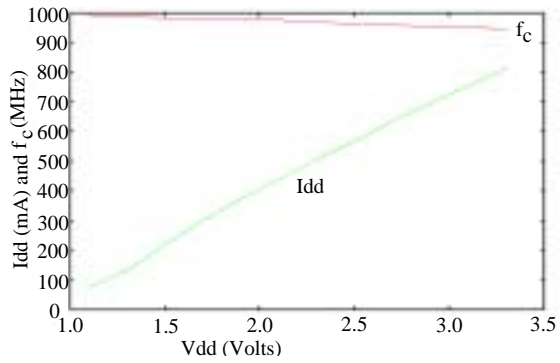


Figure 6) Clock frequency vs. Vdd for the large ring and Idd vs. Vdd for the entire chip with all six rings.

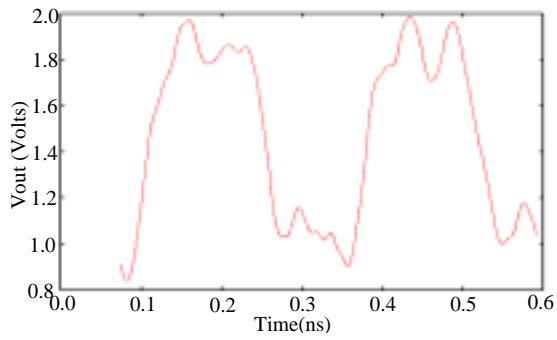


Figure 7) Measured output on one of the 3.42 GHz rings.