

Figure 1. An FPGA can implement all the necessary blocks to close the loop around the MPS14 dual synthesizer. Dual outputs on each MPS14 synthesizer conveniently provide output clock feedback to the phase detector.

Synchronous Ethernet applications require jitter attenuators in order to clean up the recovered line clock and retransmit data using that clock. In addition to low jitter, applications sometimes require translation between frequencies that are not integer multiples of each other, for example, 155.52MHz and 156.25MHz. The MPS14 coupled with an FPGA is an ideal solution that implements a dual channel jitter attenuator with any-frequency translation. Taking advantage of the flexibility provided by the FPGA, this solution can clean two clock signals independently.

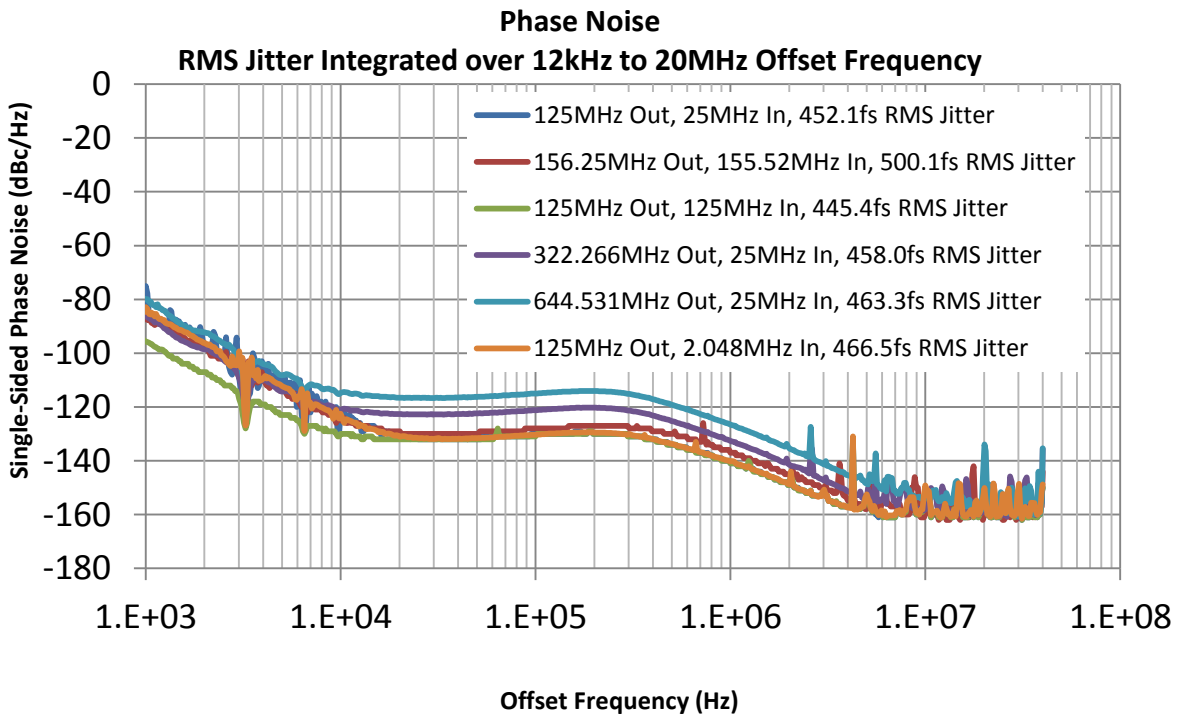


Figure 2. Ultra low-phase noise and jitter with minimal spurs across a wide frequency range makes the MPS14 an ideal solution for synchronous Ethernet applications that require optimal performance and flexibility.