

## Introduction

Digital PLLs (DPLLs) have been widely used in telecommunications systems in order to synchronize clocks, translate frequencies, and clean jitter on noisy clock signals. In order to provide maximum flexibility, DPLLs are often implemented using FPGAs for the control logic coupled with external Digital to Analog Converters (DACs) that in turn drive external analog VCXOs. The DAC is required to provide an interface between the FPGA and the VCXO. The VCXO is required to provide a clean frequency that can be adjusted (pulled). While providing acceptable performance, this DAC/VCXO combination is subject to noise and increased circuit complexity. The combination can also degrade flexibility, since most VCXOs operate at only one output frequency.

In contrast, digital clock synthesizers can be used to provide improved performance, enhanced lock range, and greater flexibility compared to VCXO based DPLLs. The use of in-circuit frequency steering allows devices such as the MPS14 to be natively controlled using a purely digital SPI bus that is programmable onto any FPGA.

## Replacing Analog VCXOs

The MPS14 features two digitally controlled synthesizers based on Rotating Traveling Wave Oscillator (RTWO) technology with DigiPull functionality. DigiPull refers to the action of steering the output frequency of the RTWO PLL using digital commands through the SPI port. These commands act on the feedback divider, not on the crystal. Since the feedback divider determines the output frequency, a single digital word can be used to make incremental

adjustments as small as 0.05 parts per billion or to generate larger frequency hops, thereby achieving exact numerical control of the output frequency.

DigiPull is the natural evolution of frequency control and offers several advantages. Generating any frequency using simple digital commands simplifies clocking applications. It eliminates the need for DACs and VCXOs in FPGA clocking applications. This reduces noise usually introduced by using data converters, reduces component count, reduces design complexity, and increases the frequency range of the end circuit.

In addition, the absence of analog pulling means that a simple non-pullable crystal can be used, whereas analog VCXOs require pullable crystals. The MPS14 uses a simple fundamental mode crystal in the range of 22MHz to 54MHz. Obsolete the pullable crystal reduces cost, helps simplify the supply chain, and increases robustness and reliability of the application.

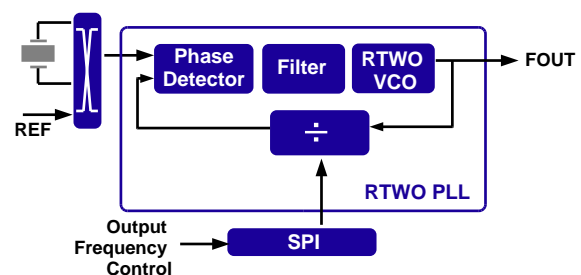


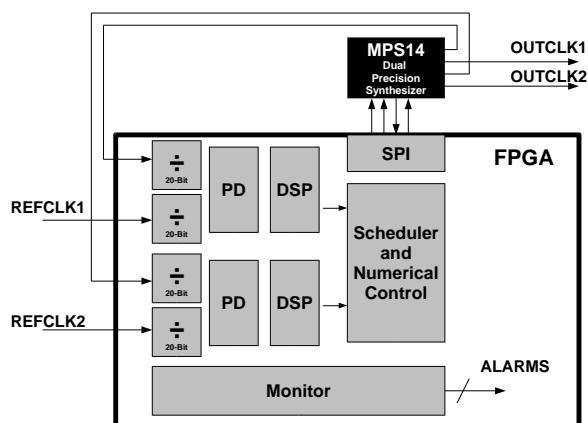
Figure 1. DigiPull within the MPS14. The output frequency of the MPS14 can be controlled with a digital word that changes the feedback divider.

## Closing the Loop: DPLL Architecture

Using an FPGA to close the loop around an MPS14 is straightforward. The architecture is similar to the VCXO-based DPLL except there is

no DAC in the system and a digital synthesizer built into the MPS14 replaces the VCXO. Since the MPS14 is a dual synthesizer, the implementation naturally implements a dual channel DPLL using only a single external IC. This offers channel density advantages compared to using two single channel VCXOs plus a dual channel DAC. One MPS14 coupled with a simple crystal can replace multiple components (two DACs and two VCXOs).

The implementation within the FPGA looks similar to any DPLL (see Figure 2). There is a phase detector (PD) followed by a DSP loop filter that sculpts the jitter transfer response and determines the bandwidth of the closed loop. The best performance will be achieved using a high resolution PD. For optimal performance, some care is necessary when placing and routing the PD within the FPGA.



**Figure 2.** An FPGA can implement all the necessary blocks to close the loop around the MPS14 dual synthesizer. Dual outputs on each MPS14 synthesizer conveniently provide output clock feedback to the phase detector.

The rest of the blocks are digital in nature and require little attention when placing and routing. The scheduler is necessary because there are two loops operating concurrently on a

single SPI bus. There is also numerical scaling that controls the gain response of the DPLL.

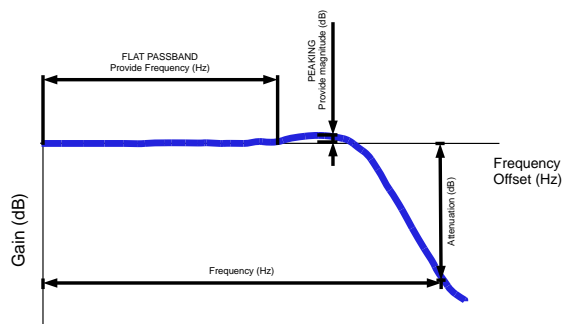
The REFCLK to OUTCLK frequency relationship is controlled using input dividers on the REFCLK frequency and the feedback signal. For instance, an input to output ratio of 255/237 that enables forward error correction applications common in optical links can be achieved by setting the REFCLK divider to a multiple of 237 and the feedback divider to the same multiple of 255. This achieves exact translation with 0ppm error from input to output. Translation between 1000/1001 can also be implemented using the input dividers. Simpler translations (1/1 or 1/5) required by applications such as synchronous Ethernet can also be achieved.

## Improved Total System Robustness

One of the most dramatic differences between a DPLL and an analog PLL is the enhanced capabilities achieved using numerical control. With analog PLLs, a time continuous voltage or current drives the VCXO control input that determines the output frequency. In that analog domain, it is difficult to freeze the value, manipulate it mathematically, or open the loop to block the influence of the reference clock to the output. In contrast, any of these functions are easily implemented in the digital domain using exact numerical control. Clock monitoring and alarms for loss of signal, loss of clock, or loss of PLL lock can be implemented.

## Jitter Transfer

The basic role of the DPLL is to track the input frequency accurately while attenuating jitter. The jitter transfer function is an important figure of merit for any DPLL. The objective is to achieve a flat passband, low loop bandwidth, low peaking and large attenuation after the roll-off. Several parameters are inter-related to generate the shape of the transfer function. Figure 3 describes a typical transfer function curve.



**Figure 3.** The configurable DSP filter allows shaping of the jitter transfer curve to target optimal passband, peaking and attenuation for each application.

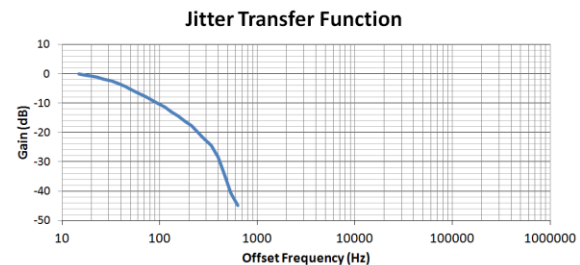
The passband defines how well the DPLL tracks the input frequency. The DPLL should be able to follow slow changes in frequency, referred to as wander. Wander (phase noise below 10Hz offset from the carrier) does not affect bit error rate and passes benignly through the DPLL.

Although all PLLs attenuate some jitter, jitter attenuators specifically refer to PLLs that have very low loop bandwidths such that they attenuate high frequency phase noise on the reference clock signal. In the analog domain, low loop bandwidths require large, bulky, fixed frequency analog components. Replacing those with a digital filter allows very low bandwidths without large passive components. And the

bandwidth can be easily changed by changing filter coefficients. In contrast, analog filters require a change to the bill of materials each time the bandwidth is changed.

Another important metric is the peaking and the roll-off. Generally, the steeper the roll-off, the greater the peaking. Low peaking (less than 0.1dB) is important when multiple PLLs will be cascaded together. This is the case in many telecom systems. Higher order digital filters can help precisely sculpt the roll-off and peaking. Figure 4 shows the jitter transfer function achieved with the MPS14-based DPLL. Since the DSP filter coefficients are programmable, many other transfer functions are possible at higher or lower cut-off frequencies and with different peaking profiles.

In this example, peaking remains lower than 0.1dB and a -3dB bandwidth of 35Hz can be achieved with a steep attenuation near 40dB at 500Hz. The roll-off continues at -60dB/decade, although it cannot be easily measured beyond 600Hz. This means that reference clock noise beyond 500Hz will be steeply attenuated. By 1kHz, the reference signal has no perceptible influence on the output.



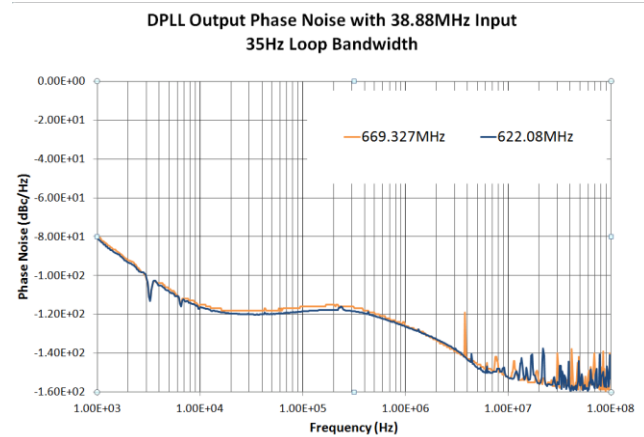
**Figure 4.** A flexible DSP based filter controls the shape of the jitter transfer curve. Low peaking and steep -60dB/decade roll-off are achievable using this DPLL design.

## 400fs Output Jitter Improves BER

System bit error rate is strongly dependent on jitter not affected by wander. For this reason, communications protocols specify integration bands typically greater than 10kHz offset from the carrier. For OC-48, jitter is integrated over 12kHz to 20MHz offsets. For OC-192, the band is 50kHz to 80MHz. The closed loop response of the DPLL rejects reference clock noise beyond 1kHz offset. Therefore, the output jitter depends primarily on the ultra-low jitter performance of the MPS14, not the DPLL loop.

Analog VCXOs typically have a control bandwidth of 50kHz or higher. This allows analog noise from the DAC or other parts of the system to influence the output in the critical bands of 12kHz to 20MHz or 50kHz to 80MHz. A DPLL using the MPS14 does not inject extra noise in these bands.

Figure 5 shows an example of the output phase noise with two output frequencies, one representing a base SONET/SDH frequency and the other representing that frequency with a 255/237 FEC scaling factor. Since the MPS14 exhibits ultra-low phase noise across any frequency, it can be used to numerically lock it to any input rate, including rational FEC rates up to 938MHz, while maintaining excellent output jitter performance. The FPGA loop has complete control of the output frequency and can lock it to any input frequency.



**Figure 5. Ultra-low MPS14 jitter and sharp DPLL roll-off means that the output jitter of the DPLL will always be clean with any reasonable clock signal.**

Table 1 summarizes the output jitter results. In the band of interest for telecom applications, the DPLL adopts the ultra-low output jitter of the MPS14 with output jitter typically varying between 350fs and 450fs for any frequency.

**Table 1. Output jitter of DPLL is governed by the low intrinsic jitter of MPS14, typically between 350fs and 450fs.**

	12kHz to 20MHz	50kHz to 80MHz
<b>MPS14 Intrinsic Jitter (622.08MHz)</b>	368.8fs	370.9fs
<b>MPS14 Intrinsic Jitter (669.327MHz)</b>	412.4fs	414.7fs
<b>DPLL Jitter (622.08MHz)</b>	374.0fs	375.1fs
<b>DPLL Jitter (669.327MHz)</b>	423.3fs	423.6fs

## Conclusion

MPS14-based DPLLs can easily exceed the performance of analog VCXOs while increasing flexibility and total system robustness.